

**Shukri J. Souri, Ph.D.**  
**Principal and Office Director, New York**

**Professional Profile**

Dr. Shukri Souri is a Principal in Exponent's Electrical and Semiconductors practice and is the Director of the New York office. Dr. Souri's background is in electrical and electronic engineering and computer systems. His professional activities include addressing issues related to electrical components, semiconductors, integrated circuits (ICs), electronics and software. His specialties include intellectual property analysis, manufacturing, reliability and failure analysis of electronic products and assemblies, medical devices, optical systems, computer memories, circuit protection, computer communications, networks and software.

Dr. Souri received his Ph.D. in Electrical Engineering at Stanford University on 3-Dimensional integration of ICs and has taught several courses on IC fabrication, optical fiber communications, TCP/IP networking, and communications protocols and implementation of systems on 3-D chips. His research interests include: solid state light emitting devices; semiconductor materials, devices and fabrication processes; microprocessor architecture and circuit design; audio/video/image processing software and content delivery technologies; medical devices including resectoscopes, cochlear implants and ICDs; embedded controls systems for computer hard disk drives; IC packaging and printed circuit board assembly; telephony, mobile communications and networking.

**Academic Credentials and Professional Honors**

Ph.D., Electrical Engineering, Stanford University, 2003  
M.S., Electrical Engineering, Stanford University, 1994  
M.A., Oxford University (U.K), 2007  
B.A. (Honors), Engineering Science, Oxford University (U.K.), 1992

## Patents

Patent 6,188,556: Two-Terminal Transistor PTC Circuit Protection Devices, WO0024126, 2001 (with C. McCoy, H. Duffy, A. Cogan, and R. Bommakant).

Patent 6,181,541: Transistor-PTC Circuit Protection Devices, WO0024105, 2001 (with H. Duffy, A. Cogan, M. Munch, and N. Nickols).

Patent 6,153,948: Electronic Circuits with Wide Dynamic Range of On/Off Delay Time, WO001249, 2000 (with A. Cogan).

Patent 5,569,495: Method of Making Varistor Chip with Etching to Remove Damaged Surfaces, CA2220931, EP0826225, WO963978, JP11505375T, 1996 (with A. Evans, T. Tsukada, and R. Dupon).

## Publications

Fu J, Souri S, Harris J. Temperature and humidity dependent reliability analysis of RGB LED chip. Proceedings, ISTFA 2006: Discrettes, Passives, MEMS, and Optoelectronics, pp. 137–141, 2006.

Saraswat K, Kapur P, Souri S. Performance limitations of metal interconnects and possible alternatives. 203<sup>rd</sup> Meeting of the Electrochemical Society, Paris, France, April 2003.

Saraswat K, Kapur P, Chandra G, Chiang T-Y, Souri S. Scaling induced performance limitations of metal interconnects. IEEE ISSCC Microprocessor Design Workshop, San Francisco, CA, February 2002.

Chiang T, Souri S, Chui C, Saraswat K. Thermal analysis of heterogeneous 3-D ICs with various integration scenarios. IEEE IEDM, December 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D Heterogeneous ICs: A technology for the next decade and beyond. 5<sup>th</sup> IEEE Workshop on Signal Propagation on Interconnects, Venice, Italy, May 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. Proceedings, IEEE: Special Issue on Interconnections, Vol. 89, No. 5, pp. 602–633, May 2001.

Davis J, Venkatesan R, Kaloyeros A, Bylansky M, Souri S, Banerjee K, Saraswat K, Rahman A, Reif R, Meindl J. Integration limits on Gigascale Integration (GSI) in the 21<sup>st</sup> Century. Proceedings, IEEE: Special Issue of Limits to Semiconductor Technology, Vol. 89, No. 3, pp. 3-05–324, March 2001.

Saraswat K, Banerjee K, Joshi A, Kalvade P, Kapur P, Souri S. 3-D ICs: Motivation, performance analysis and technology. Proceedings, 26<sup>th</sup> European Solid-State Circuits Conference (ESSCIRC), Stockholm, Sweden, September 19–21, 2000.

Souri S, Banerjee K, Mehrotra A, Saraswat KC. Multiple Si layer ICs: Motivation, performance analysis, and design implications. 37<sup>th</sup> ACM Design Automation Conference (DAC), pp. 213–220, Los Angeles, CA, June 5–9, 2000.

Saraswat K, Banerjee K, Joshi A, Kalavade P, Souri S, Subramanian V. 3-D ICs with multiple Si Layers: Performance analysis, and technology. 5<sup>th</sup> International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues, 197<sup>th</sup> Meeting of the Electrochemical Society, Toronto, Canada, May 14–19, 2000.

Saraswat K, Souri S, Subramanian V, Joshi A, Wang A. Novel 3-D structures. Proceedings, IEEE International SOI Conference, pp. 54–55, 1999.

Subramanian V, Toita M, Ibrahim N, Souri S, Saraswat K. Low-leakage germanium-seeded laterally-crystallized single-grain 100nm TFTs for vertical integration applications. IEEE Electron Device Letters, Vol. 20, pp. 341–343, 1999.

Souri S, Saraswat K. Interconnect performance modeling for 3D integrated circuits with multiple Si layers. IEEE International Interconnect Technology Conference, pp. 24–26, 1999.

Haskell B, Souri S, Helfand M. Varistor behavior at twin boundaries in ZnO. Journal of the American Ceramic Society, Vol. 82, No. 8, August 1999.

Chu A, Souri S, Melfand M, Kinsman K, Dupon R. Superior electrical performance of Raychem ZnO Varistor through advanced processing. Proceedings, 1<sup>st</sup> Asian Meeting on Ferroelectricity, Xian, China, October 5–8, 1995.

### **Book Chapters**

Souri S, Chiang T, Kapur P, Banerjee K, Saraswat KC. 3-D ICs deep submicron interconnect performance modeling and analysis. In: Interconnect Technology and Design for Gigascale Integration. Davis J and Meindl J (eds), Kluwer Academic Publishers, October 2003.

### **Speaker Engagements**

Souri S. 3-Dimensional ICs interconnect architecture, technology and performance analysis. Oral Defense, Stanford University, 2003.

Souri S. 3-D ICs with multiple Si Layers: performance analysis and technology. Solid State Technology and Devices Seminar, Microlab, UC Berkeley, 2001.

Souri S. 3D ICs: Performance, analysis and technology. Integrated Circuits and Technology Seminar, Stanford University, 2001.

Souri S. Photorefractance microscopy of semiconductor materials. Raychem Corporation, CR&D, Menlo Park, CA, 1994.

### **Prior Experience**

Founder, Merenga Inc., 2000–2002

Co-Founder and Engineering Manager, arcadiaOne, Inc., 1999–2000

Research Engineer, Circuit Protection Division, Raychem, 1996–1997

Research Scientist, Corporate Research & Development, Raychem, 1994–1996

### **Professional Affiliations**

- Institute of Electrical and Electronic Engineers (member)
- Oxford University Society (life member)
- Oxford Union (member)