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Professional Profile

Dr. Melvin has extensive experience across many areas in electronics and computing systems including processor architecture, memory systems, network processing, digital communications and embedded systems. His professional activities primarily involve advising industrial and legal clients relating to intellectual property.

Dr. Melvin received his Ph.D. in Computer Science at the University of California at Berkeley on a high-performance processor design that exploited fine-grained parallelism in general purpose programs. He led an RTL architecture team designing a network processor utilizing a simultaneous multithreading architecture, and he was a co-founder of a second network processor startup that developed a massively multithreaded processor for deep packet inspection on edge routers. Dr. Melvin has also designed and built numerous real-time embedded systems that have been commercially deployed, including machine vision systems used in the automotive industry and voice processing systems.

In the intellectual property area Dr. Melvin has wide-ranging experience as a consulting and testifying expert in patent, copyright and trade secret litigation. He has acted as a court appointed expert, as an in-house technical expert at a large international law firm and he is also a patent agent registered with the USPTO. Dr. Melvin has offered expert testimony in a wide range of technology areas including CPU microarchitecture, memory systems, voice and image processing, wireless communications, networking systems, computer aided design tools, security software, data compression, programmable logic devices, flash memory technology and hard disk drive architectures.

Academic Credentials & Professional Honors

Ph.D., Computer Science, University of California, Berkeley, 1991

B.S., Electrical Engineering and Computer Science, University of California, Berkeley, 1982

Licenses and Certifications

Patent Agent, USPTO, #50467

Academic Appointments

General Chair, 45th Annual Symposium in Microarchitecture (MICRO-45), Vancouver, British Columbia, December 2012.

Visiting Scholar, University of Texas, Austin, September 2001 – April 2002.

Co-Chair, 29th Annual Symposium in Microarchitecture (MICRO-29), Paris, France, December 1996.

Prior Experience

Technical Advisor, O'Melveny & Myers, 2002 - 2005.

Co-Founder, Flowstorm, Inc. (later Consentry networks), 2001 - 2002.

Senior Architect, Clearwater Networks (formerly XStream Logic, Inc.), 2000 - 2001.

Professional Affiliations

The Institute of Electrical and Electronics Engineers (IEEE), Member.

The Association for Computing Machinery (ACM), Member.

The American Intellectual Property Law Association (AIPLA), Member.

Patents

US Patent 6,922,138: Vehicle Specific Messaging Apparatus and Method, July, 2005.

US Patent 6,981,110: Hardware Enforced Virtual Sequentiality, December, 2005.

U.S. Patent 7,035,998: Clustering Stream and/or Instruction Queues for Multi-Streaming Processors, April, 2006 (M. Nemirovsky, N. Sampath, E. Musoll, H. Urdaneta).

US Patent 7,042,887: Method and Apparatus for Non-Speculative Pre-Fetch Operations in Data Packet Processing, May, 2006 (N. Sampath, E. Musoll, M. Nemirovsky).

US Patent 7,058,064: Queueing System for Processors in Packet Routing Operations, June, 2006 (M. Nemirovsky, E. Musoll, N. Sankar, N. Sampath, A. Nemirovsky).

US Patent 7,065,096: Method for Allocating Memory Space for Limited Packet Head and/or Tail Growth, June, 2006 (E. Musoll, M. Nemirovsky).

US Patent 7,107,402: Packet Processor Memory Interface, September, 2006.

US Patent 7,139,901: Extended Instruction Set for Packet Processing Applications, November, 2006 (E. Musoll, M. Nemirovsky).

US Patent 7,155,516: Method and Apparatus for Overflowing Data Packets to a Software-Controlled Memory When They Do Not Fit Into a Hardware-Controlled Memory, December, 2006 (E. Musoll, M. Nemirovsky).

US Patent 7,165,257: Context Selection and Activation Mechanism for Activating One of a Group of Inactive Contexts in a Processor Core for Servicing Interrupts, January, 2007 (E. Musoll, M. Nemirovsky).

US Patent 7,197,043: Method for Allocating Memory Space for Limited Packet Head and/or Tail Growth, March, 2007 (E. Musoll, M. Nemirovsky).

US Patent 7,257,814: Method and Apparatus for Implementing Atomicity of Memory Operations in Dynamic Multi-Streaming Processors, August, 2007 (M. Nemirovsky).

US Patent 7,280,548: Method and Apparatus for Non-speculative Pre-fetch Operation in Data Packet Processing, October, 2007 (N. Sampath, E. Musoll, M. Nemirovsky).

US Patent 7,319,379: Profile-Based Messaging Apparatus and Method, January, 2008.

US Patent 7,346,710: Apparatus for Input/Output Expansion Without Additional Control Line Wherein First and Second Signals Transition Directly to a Different State When Necessary to Perform Input/Output, March, 2008.

US Patent 7,360,217: Multi-Threaded Packet Processing Engine for Stateful Packet Processing, April, 2008 (M. Nemirovsky, E. Musoll, J. Huynh).

US Patent 7,441,088: Packet Processor Memory Conflict Prediction, October, 2008.

US Patent 7,444,481: Packet Processor Memory Interface With Memory Conflict Value Checking, October, 2008.

US Patent 7,475,200: Packet Processor Memory Interface With Write Dependency List, January, 2009.

US Patent 7,475,201: Packet Processor Memory Interface With Conditional Delayed Restart, January, 2009.

US Patent 7,478,209: Packet Processor Memory Interface With Conflict Detection And Checkpoint Repair, January, 2009.

US Patent 7,482,910: Apparatus, System, and Computer Program Product for Presenting Unsolicited Information to a Vehicle or Individual, January, 2009.

US Patent 7,487,304: Packet Processor Memory Interface With Active Packet List, February, 2009.

US Patent 7,496,721: Packet Processor Memory Interface With Late Order Binding, February, 2009.

US Patent 7,506,104: Packet Processor Memory Interface With Speculative Memory Reads, March, 2009.

US Patent 7,529,907: Method and Apparatus for Improved Computer Load and Store Operations, May, 2009 (M. Nemirovsky, E. Musoll, N. Sankar).

US Patent 7,551,626: Queueing System for Processors in Packet Routing Operations, June, 2009 (M. Nemirovsky, E. Musoll, N. Sankar, N. Sampath, A. Nemirovsky).

US Patent 7,606,942: Method for Input Output Expansion in an Embedded System Utilizing Controlled Transitions of First and Second Signals, October, 2009.

US Patent 7,650,605: Method And Apparatus For Implementing Atomicity Of Memory Operations In Dynamic Multi-streaming Processors, January, 2010 (M. Nemirovsky).

US Patent 7,668,954: Unique Identifier Validation, February, 2010.

US Patent 7,715,410: Queueing System for Processors in Packet Routing Operations, May, 2010 (M. Nemirovsky, E. Musoll, N. Sankar, N. Sampath, A. Nemirovsky).

US Patent 7,739,452: Method and Apparatus for Hardware Enforced Virtual Sequentiality, June, 2010.

US Patent 7,765,554: Context Selection and Activation Mechanism for Activating One of a Group of Inactive Contexts in a Processor Core for Servicing Interrupts, July, 2010 (E. Musoll, M. Nemirovsky).

US Patent 7,876,427: Headlamp Alignment Detection Using A Network Of Independent Sensor Units, January, 2011.

US Patent 7,877,481: Method And Apparatus For Overflowing Data Packets To A Software-Controlled Memory When They Do Not Fit Into A Hardware-Controlled Memory, January, 2011 (E. Musoll, M. Nemirovsky).

US Patent 8,004,663: Headlamp Aim Detection With Sensors Independent From Host Control Unit, August, 2011.

US Patent 8,131,882: Method for Input Output Expansion in an Embedded System Utilizing Controlled Transitions of First and Second Signals, March, 2012.

US Patent 8,184,275: Vehicle Headlamp Monitoring Using A Network Accessible User Interface, May, 2012.

US Patent 8,214,482: Remote Log Repository With Access Policy, July, 2012.

US Patent 8,275,996: Incremental Encryption Of Stored Information, September, 2012.

US Patent 8,301,753: Endpoint Activity Logging, October, 2012.

US Patent 8,307,072: Network Adapter Validation, November, 2012.

US Patent 8,429,420: Time-Based Key Management For Encrypted Information, April, 2013.

US Patent 8,732,482: Incremental Encryption Of Stored Information, May, 2014.

US Patent 8,806,066: Method for Input Output Expansion in an Embedded System Utilizing Controlled Transitions of First and Second Signals, August, 2014.

US Patent 8,812,875: Virtual Self-Destruction Of Stored Information, August, 2014.

US Patent 8,917,190: Method of Restricting Turns at Vehicle Intersections, December, 2014.

US Patent 9,245,155: Virtual Self-Destruction of Stored Information, January, 2016.

US Patent 10,051,555: User Specific Access Throttler For Access Points, August, 2018.

Publications

Patt, Y., Hwu, W., Melvin, S., and Shebanow, M., "HPS Papers: A Retrospective," IEEE Micro July/August 2016, vol. 36, no. 4, pp. 76-79.

Melvin, S., "Endpoint Identification Using System Logs", Workshop on the Analysis of System Logs (WASL) 2009, held in conjunction with the 22nd ACM Symposium on Operating System Principles (SOSP), Big Sky, Montana, October 2009.

Melvin, S., Nemirovsky, M., Musoll, E., Huynh, J., Milito, R., Urdaneta, H., and Saraf, K., “A Massively Multithreaded Packet Processor,” NP2: Workshop on Network Processors, held in conjunction with The 9th International Symposium on High-Performance Computer Architecture (HPCA-9), Anaheim, California, February 8-9, 2003.

Melvin, S. and Patt, Y., “Handling of Packet Dependencies: A Critical Issue for Highly Parallel Network Processors,” Proceedings, International Conference on Compilers, Architectures, and Synthesis for Embedded Systems, October 8 – 11, 2002.

Melvin, S., and Patt, Y., “Enhancing Instruction Scheduling with a Block-Structured ISA,” International Journal of Parallel Processing, 23(3):221-243, 1995.

Melvin, S., and Patt, Y., “Exploiting Fine-grained Parallelism Through a Combination of Hardware and Software Techniques,” Proceedings, 18th International Symposium on Computer Architecture, Toronto, Canada, May 1991.

Melvin, S., and Patt, Y., “Performance Benefits of Large Execution Atomic Units in Dynamically Scheduled Machines,” Proceedings, 1989 Supercomputer Conference, Crete, Greece, June 1989.

Melvin, S., Shebanow, M., and Patt, Y., “Hardware Support for Large Atomic Units in Dynamically Scheduled Machines,” Proceedings, 21st Annual Workshop on Microprogramming and Microarchitecture, San Diego, California, November 1988.

Melvin, S., and Patt, Y., “The Use of Microcode Instrumentation for Development, Debugging and Tuning of Operating System Kernels,” Proceedings, 1988 ACM SIGMETRICS, Santa Fe, New Mexico, May 1988.

Melvin, S., and Patt, Y., “A Clarification of the Dynamic/Static Interface,” Proceedings, 20th Hawaii International Conference on System Sciences, Kailua-Kona, Hawaii, January 1987.

Gee, J., Melvin, S., and Patt, Y., “Advantages of Implementing Prolog by Microprogramming a General Purpose Host Computer,” Proceedings, Fourth International Conference on Logic Programming, Melbourne, Australia, May 1987.

Melvin, S., and Patt, Y., “SPAM: A Microcode Based Tool for Tracing Operating System Events,” Proceedings, 20th Annual Workshop on Microprogramming, Colorado Springs, Colorado, December 1987.

Melvin, S., Wilson, J., Shebanow, M., Hwu, W. and Patt, Y., “On Tuning the Microarchitecture of an HPS Implementation of the VAX,” Proceedings, 20th Annual Workshop on Microprogramming, Colorado Springs, Colorado, December 1987.

Melvin, S., and Patt, Y., “A Microcode-Based Environment for Non-invasive Performance Analysis,” Proceedings, 19th Annual International Workshop on Microprogramming, New York, October 1986.

Gee, J., Melvin, S., and Patt, Y., “The Implementation of Prolog via VAX 8600 Microcode,” Proceedings, 19th Annual Workshop on Microprogramming, New York, October 1986.

Patt, Y., Melvin, S., Hwu, W., Shebanow, M., Chien, C., and Wei, J., “Run-Time Generation of HPS Microinstructions from a VAX Instruction Stream,” Proceedings, 19th Annual Workshop on Microprogramming, New York, October 1986.

Patt, Y., Hwu, W., Melvin, S., Shebanow, M., Chien, C., and Wei, J., “An HPS Implementation of VAX: Initial Design and Analysis,” Proceedings, 19th Hawaii International Conference on System Sciences, Honolulu, Hawaii, January 1986.

Patt, Y., Shebanow, M., Hwu, W., and Melvin, S., “A C Compiler for HPS I, A Highly Parallel Execution Engine,” Proceedings, 19th Hawaii International Conference on System Sciences, Honolulu, Hawaii, January 1986.

Patt, Y., Melvin, S., Hwu, W., and Shebanow, M., “Critical Issues Regarding HPS, A High Performance Microarchitecture,” Proceedings, 18th Annual Workshop on Microprogramming, Asilomar, California, December 1985.